2811

Attorney Docket No. 03692.P054D2

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:		
DISNEY, D.	Examiner:	Loke, Steven Ho Yin
Serial No.: 10/647,925	Art Unit:	2811
Filing Date: August 26, 2003		
For: High-Voltage Transistor With Buried Conduction Layer		

Information Disclosure Statement

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Enclosed is a copy of Information Disclosure Citation Form PTO-1449A together with a copy of the documents cited on that form. It is respectfully requested that the cited documents be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449A be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

Pursuant to 37 C.F.R. § 1.97, this Information Disclosure Statement is being submitted under one of the following (as indicated by an "X" to the left of

Form PTO-1449 (Modified)	Atty Docket No.: 03692.P054D2	Serial No.: 10/647,925
List of Patents and Publications Statement (Use several sheets if necessary)	Applicants: Disney, D.	
	Filing Date: August 26,2003	

REFERENCE DESIGNATION				U.S. PATENT DOCUMENTS			
Exam. Initial		Date	Document Number	Name	Class	Sub-Class	Filing Date

FOREIGN PATENT DOCUMENTS

No.		Document No.	Date	Country	Name	Class	Sub-Class	Trans-lation
		JP 3-211771	09/17/91	Japan	Toshiba			English
		JP 4-107867	04/09/92	Japan	Yamanishi, et al.			English
		JP 57-12558	01/22/82	Japan	Tanaka, et al.			English
		WO 99/34449	07/08/99	PCT	Letavic, et al.			

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

		"Air-Gap Formation During IMD Deposition to Lower Interconnect Capacitance," B. Shieh, et al., IEEE Electron Device Letters, Vol. 19, No. 1, January 1998.
		"Oxide-Bypassed VDMOS (OBVDMOS): An Alternative to Superjunction High-Voltage MOS Power Devices," Yung C. Liang, et al., IEEE Electron Device Letters, Vol. 22, No. 8, August 8, 2001, Pages 407-409.
		"Comparison of High-Voltage Devices for Power Integrated Circuits," R. Jayaraman, et al., IEDM 84, 1984, Pages 258-261.
		"A New Generation of High-Voltage MOSFETs Breaks the Limit Line of Silicon," G. Debby, et al., Siemens AG, Munchen, Germany, IEDM 98-683 – IEDM 98-685.

Examiner	*Date Considered*

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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No.		Document No.	Date	Country	Name	Class	Sub-Class	Trans-lation
		JP 6-224426	08/12/94	Japan	Uno			English
		DE 43 09 764	09/29/94	Germany	Tihanyi, et al.			
		JP 56-38867	04/14/81	Japan	Okabe, T., et al.			English
		JP 57-10975	01/20/82	Japan	Sanyo			English
		JP 57-12557	01/22/82	Japan	Tanaka, et al.			English
		JP 57-12558	01/22/82	Japan	Tanaka, et al.			English
		JP 60-64471	04/13/85	Japan	Saitou, M.			

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

		"International Electron Devices Meeting 1979- Washington, D.C, Dec. 3-4-5," Sponsored by Electron Devices Society of IEEE, Pages 238-241.
		"Realization of High Breakdown of Voltage (>700V) in Thin SOI Devices," S. Merchant, et al., Phillips Laboratories North America, 1991 IEEE, Pages 31-35.
		"Theory of Semiconductor Superjunction Devices," T. Fujuhana, Japanese Journal of Applied Physics, Part 1, October 1997, Vol. 36, No. 10, Pages 6254-6262.

Examiner	*Date Considered*

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REFERENCE DESIGNATION — **U.S. PATENT DOCUMENTS**

Exam. Initial		Date	Document Number	Name	Class	Sub-Class	Filing Date

FOREIGN PATENT DOCUMENTS

No.		Document No.	Date	Country Name	Class	Sub-Class	Trans-lation

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

		"High Performance 600 V Smart Power Technology Based on Thin Layer Silicon-on-Insulator," T. Letavic, et al., Phillips Electronics North America Corp., 4 Pages.
		"Modern Semiconductor Device Physics," S. M. Sze, John Wiley & Sons, 1998, Chapter 4, Pages 203-206.
		"Modeling Optimization of Lateral High Voltage IC Devices to Minimize 3-D Effects," H. Yilmaz, R&D Engineering, GE Corp., NC, Pages 290-297.

Examiner	***Date Considered***

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

the appropriate paragraph):

_____ 37 C.F.R. §1.97(b).

__XX__ 37 C.F.R. §1.97(c). If so, then enclosed with this Information Disclosure Statement is one of the following:

____ A statement pursuant to 37 C.F.R. §1.97(e) or

__XX__ A check for $180.00 for the fee under 37 C.F.R. § 1.17(p).

_____ 37 C.F.R. §1.97(d). If so, then enclosed with this Information Disclosure Statement are the following:

(1) A statement pursuant to 37 C.F.R. §1.97(e); and

(2) A check for $180.00 for the fee under 37 C.F.R. §1.17(p) for submission of the Information Disclosure Statement.

Please charge any shortages of fees or credit any overcharges of fees to our Deposit Account No. 50-2060.

Respectfully submitted,
BURGESS & BEREZNAK, LLP

Dated: 4/30, 2004

Bradley J. Bereznak
Attorney for Applicant
Registration No. 33,474

FIRST CLASS CERTIFICATE OF MAILING
(37 C.F.R. § 1.8(a))

I hereby certify that the foregoing INFORMATION DISCLOSURE STATEMENT is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on April 30, 2004 .

John Bereznak
Name of Person Mailing Correspondence

Signature

04/30/2004
Date